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10/692,687	10/27/2003	Kazuto Usuda	030712-15	2065

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EXAMINER	
ALIA, CURTIS A	

ART UNIT	PAPER NUMBER
2416	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/692,687	USUDA ET AL.	
	Examiner	Art Unit	
	Curtis A. Alia	2416	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 September 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Applicant's amendment filed on 11 March 2008 has been entered. Claim 13 has been amended. Claims 1-15 are still pending in this application, with claims 1 and 10 being independent. Please note that AU 2616 has been changed to AU 2416.

Response to Arguments

1. Applicant's arguments with respect to claims 1-2 and 4-9 have been considered but are moot in view of the new ground(s) of rejection.

2. Applicant's arguments filed 15 September 2008 with respect to claims 10-15 have been fully considered but they are not persuasive. The FIFO buffer of Jay is a single buffer with an input and an output (see figure 7, buffer 700). Haywood teaches that such a buffer can be split into three portions (head, tail, and body, see figure 1). The packet delete area corresponds to the tail FIFO memory, and the packet add area corresponds to the head FIFO memory. As claimed, the limitations of claim 10 are taught by Jay and Haywood. The tail FIFO deletes packets and places them onto the large memory, whereas the add area will add packets from packets stored in the large memory.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 6 and 9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 6 and 9 depend from claim 3, which is a cancelled claim. It is suggested that claims 6 and 9 be cancelled, since the same limitations are presented in claims 5 and 8.

Claim Rejections - 35 USC § 103

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jay et al. (previously cited US 6,400,683) in view of Haywood (previously cited US 6,987,775) and Oldak et al. (newly cited US 7,085,236).

Regarding claim 1, Jay discloses a method of controlling a jitter buffer using a FIFO comprising the steps of setting a clock control area (see figure 7, local clock frequency generator) inside the FIFO, controlling a stored packet quantity of the FIFO to delete a specified packet when the stored packet quantity exceeds a lower limit of the FIFO buffer (see figure 7, counter 703 controls and keeps track of the stored packet quantity), raising a clock frequency when the stored packet quantity of the FIFO reaches an upper limit of the clock control area (see column 4, lines 45-47, clock is increased when buffer fills up), lowering the clock frequency

when the stored packet quantity of the FIFO reaches a lower limit of the clock control area (see column 4, lines 47-49, clock is decreased when buffer is emptying), and setting the clock control area between both ends of the FIFO buffer (see figure 7, clock area is connected through buffer monitor between both detection circuits on either side of the FIFO buffer).

Jay does not explicitly teach setting a packet delete area and a packet add area and to always delete the packets when the stored packet quantity exceeds an upper limit of the packet delete area, controlling the stored packet quantity of the FIFO to add a specified packet when the stored packet quantity falls below an upper limit of the packet add area, and to always add the packets when the stored packet quantity falls below a lower limit of the packet add area.

However, the above-mentioned claimed limitation is well known in the art, as evidenced by Haywood. In particular, Haywood teaches the steps of setting a packet delete area and a packet add area (see column 2, lines 13-15, a head FIFO and tail FIFO are set up) and to always delete the packets when the stored packet quantity exceeds an upper limit of the packet delete area (see column 2, lines 20-22, when the tail FIFO fills up, the following incoming packets are (deleted from the tail FIFO) offloaded into a off chip buffer), controlling the stored packet quantity of the FIFO to add a specified packet (specified packet is interpreted as the next packet in the head end of the FIFO, conforming to the rules of FIFO (first in first out)) when the stored packet quantity falls below an upper limit of the packet add area and to always add the packets when the stored packet quantity falls below a lower limit of the packet add area (see column 2, lines 25-27, when the head FIFO (packet add area) begins to empty, data from the off chip memory will be added into the head FIFO).

In view of the above, having the method of Jay, then given the well-established teaching of Haywood, it would have been obvious to a person having ordinary skill in the art at the time of the invention to modify the method of Jay as taught by Haywood, since Haywood stated that a high data rate can be maintained so that memory read/write speeds do not contribute to the jitter problem introduced by delay variations of the transmission scheme/medium.

Jay and Haywood do not explicitly teach deleting a specified packet from an input side of the FIFO when the stored packet quantity exceeds a lower limit of the packet delete area.

However, the above-mentioned claimed limitation is well known in the art, as evidenced by Oldak. In particular, Oldak teaches deleting a specified packet from an input side of the FIFO when the stored packet quantity exceeds a lower limit of the packet delete area (see column 5, lines 17-31, the drop-tail scheme deletes packets from the input (tail) side of the FIFO buffer when a limit has been exceeded that indicates that the FIFO buffer is saturated (lower limit).

In view of the above, having the method of Jay and Haywood, then given the well-established teaching of Oldak, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method of Jay and Haywood as taught by Oldak, since Oldak stated that the drop-tail method is a well known method for controlling the flow of packets into a buffer.

Regarding claim 2, Jay discloses that the lower limit of the packet add area is equal to the upper limit thereof (see figure 7, FIFO buffer 700 contains a packet add area where the upper limit and the lower limit are coincident (occupying the same place), meaning that the packet add area has a size of zero, essentially rendering the packet add area nonexistent).

Regarding claims 4-6, Jay discloses that the lowering of the clock frequency is linear from the upper limit of the clock control area to the lower limit thereof, and the raising of the clock frequency is linear from the lower limit of the clock control frequency to the upper limit thereof (see column 4, lines 40-49, the clock adjustment method is based on the fill level of the buffer, so the clock frequency is increased in proportion to the fill level of the buffer, and the clock frequency is decreased in proportion to how empty the buffer is).

3. Claims 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jay in view of Haywood and Oldak as applied to claims 1-3 above, and further in view of Tokura et al. (previously cited US 5,400,329).

Regarding claims 7-9, Jay, Haywood and Oldak do not explicitly teach that the lowering of the clock frequency is exponential from the upper limit of the clock control area to the lower limit thereof, and the raising of the clock frequency is exponential from the lower limit of the clock control area to the upper limit thereof.

However, the above-mentioned claimed limitation is well known in the art, as evidenced by Tokura. In particular, Tokura teaches that the lowering of the clock frequency is exponential from the upper limit of the clock control area to the lower limit thereof (see column 5, lines 15-37, when congestion is about to occur, the transmission rate can be reduced exponentially, and the rate decrease threshold is set by upper and lower limits), and the raising of the clock frequency is exponential from the lower limit of the clock control area to the upper limit thereof

(see column 5, lines 54-65, the transfer rate can be increased exponentially in the same manner as the decrease in transfer rate).

In view of the above, having the method of Jay, Haywood and Oldak, then given the well-established teaching of Tokura, it would have been common sense to one of ordinary skill in the art to modify the method of Jay, Haywood and Oldak as taught by Tokura, since Tokura stated in column 2, lines 54+ that congestion can be avoided without discarding packets.

4. Claims 10 and 12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jay in view of Haywood and Suzuki et al. (previously cited US 2002/0009054).

Regarding claim 10, Jay discloses a device of controlling a jitter buffer comprising a FIFO, having an input side and an output side, that configures the jitter buffer (see figure 7, FIFO 700), and a jitter buffer control circuit that includes a buffer accumulation level surveillance that monitors a stored packet quantity accumulated in the FIFO (see figure 7, buffer counter 703 and buffer control circuit comprising comparators 712 and 713, state machine 711), a VCO that supplies to vary a reproduced clock frequency (see figure 7, local clock frequency generator with increment/decrement circuit 706), and a buffer control circuit for controlling the operations of the FIFO and peripheral circuits thereof (see figure 7, state machine), wherein the buffer control circuit controls the quantity of packets accumulated in the FIFO to delete packets when the stored packet quantity exceeds a lower limit of the FIFO (see column 4, lines 47-49, when the buffer tends to be empty, the frequency clock is reduced, thereby controlling the quantity of packets maintained in the buffer), and the buffer control circuit controls to add the packets when

the stored packet quantity falls below an upper limit of the FIFO (see column 4, lines 45-47, when the buffer tends to be full, the frequency clock is increased, thereby controlling the quantity of packets maintained in the buffer).

Jay does not explicitly teach that the device further comprises a packet deletion circuit provided on the input side of the FIFO and a packet addition circuit provided on the output side of the FIFO.

However, the above-mentioned claimed limitation is well known in the art, as evidenced by Haywood. In particular, Haywood teaches a packet deletion circuit provided on the input side of the FIFO (see figure 1, tail FIFO 16 directly connected to receiver 11) and a packet addition circuit provided on the output side of the FIFO (see figure 1, head FIFO 17 connected to switching elements (outputs)).

In view of the above, having the device of Jay, then given the well-established teaching of Haywood, it would have been obvious to a person having ordinary skill in the art at the time of the invention to modify the device of Jay as taught by Haywood, since Haywood stated that a high data rate can be maintained so that memory read/write speeds do not contribute to the jitter problem introduced by delay variations of the transmission scheme/medium.

Jay and Haywood do not explicitly teach that the jitter buffer controller further comprises a decoder that accepts the packets outputted from the packet addition circuit and decodes frames of the packets based on the clock frequency supplied from the VCO.

However, the above-mentioned claimed limitation is well known in the art, as evidenced by Suzuki. In particular, Suzuki teaches a decoder that accepts the packets outputted from the packet addition circuit and decodes frames of the packets based on the clock frequency supplied

from the VCO (see figure 2, voice decoder 110 connected to delay unit 103 with input clock frequency from internal clock generator 107).

In view of the above, having the device of Jay and Haywood, then given the well-established teaching of Suzuki, it would have been obvious to a person having ordinary skill in the art at the time of the invention to modify the device of Jay and Haywood as taught by Suzuki, since Suzuki stated that the packets are only useful to the user if they are properly decoded (in this case, a voice decoder is needed to decode the packets into audible signals outputted to a speaker).

Regarding claim 12, Jay and Haywood teach that the jitter buffer control circuit is in direct communication with the packet deletion circuit and the packet addition circuit. As stated in the rejection of claim 10, Jay's detection circuits can be modified to include buffers for add and delete circuits, which are directly connected to the jitter buffer control circuit (see figure 7 of Jay, detection circuits 701 and 702 are connected to the buffer control circuits through the up/down counter 703)

Regarding claim 13, Jay and Haywood teach that the packet deletion circuit and the packet addition circuit are in direct communication with the buffer control circuit of the jitter buffer control circuit. As stated in the rejection Regarding claim 12, Jay's detection circuits combined with Haywood's buffers to make packet addition and deletion circuits are connected to the buffer control circuits of the jitter buffer control circuit through the up/down counter 703.

Regarding claim 14, Jay teaches that the jitter buffer control circuit is in direct communication with the jitter buffer (see figure 7, the buffer limits B_{min} and B_{max} are monitored by the buffer limit comparators 712 and 713, thus showing a direct connection between the jitter buffer and the jitter buffer control circuit).

Regarding claim 15, Jay teaches that the jitter buffer is in direct communication with a buffer monitoring portion of the jitter buffer circuit (see figure 7, the buffer limits B_{min} and B_{max} are monitored by the buffer limit comparators 712 and 713 (buffer monitoring portion), thus showing a direct connection between the buffer monitoring portion and the jitter buffer control circuit).

5. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jay in view of Haywood and Suzuki as applied to claim 10 above, and further in view of Oltean (previously cited US 6,044,113).

Regarding claim 11, Jay, Haywood and Suzuki fail to teach that a pulse width modulator is used as a replacement for the VCO.

However, the above-mentioned claimed limitation is well known in the art, as evidenced by Oltean. In particular, Oltean teaches that a pulse width modulator is used as a replacement for the VCO (see abstract, pulse width modulator produces a clock signal).

In view of the above, having the device of Jay, Haywood and Suzuki, then given the well-established teaching of Oltean, it would have been obvious to a person having ordinary skill

in the art at the time of the invention to modify the device of Jay, Haywood and Suzuki as taught by Oltean, since Oltean stated that the pulse widths of the highs and lows of the clock signals can be varied independently.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Curtis A. Alia whose telephone number is (571) 270-3116. The examiner can normally be reached on Monday through Friday, 9am-6pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Aung S. Moe can be reached on (571) 272-7314. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Aung S. Moe/
Supervisory Patent Examiner, Art Unit 2416

/Curtis A Alia/
Examiner, Art Unit 2416
12/23/2008

CAA